Remarks

Claims 1–5, 7–14, and 21–30 are pending in this application. Claims 2–5 and 8 have been amended in response to the office action. The amended claims are fully supported by the specification. No new matter has been added.

Claim Objections

Claims 2–5 and 8 have been amended to provide proper antecedent basis. The examiner's objection to these claims should be withdrawn.

Section 102 and 103 Rejections

Claims 1–2, 5–11, 13–16, and 18–20 were rejected under section 102(e) as being unpatentable by U.S. patent application publication 20060080630 (Lin). Claim 23 was rejected under section 103(a) as being unpatentable by Lin in view of Balakrishnan et al. ("A Greedy Router with Technology Targetable Output"). Claims 24–25 were rejected under section 103(a) as being unpatentable by Lin in view of U.S. patent 5,737,580 (Hathaway). Claim 30 was rejected under section 103(a) as being unpatentable by Lin in view of U.S. patent 6,109,775 (Tripathi). Reconsideration of the rejections and allowance of the claims are respectfully requested.

Claim 1 recites "a shape-based *automatic router tool*, capable of accessing the database, *using flood operations to create an interconnect route path for at least one net of the integrated circuit design*, selected using the graphical user interface tool and the mouse, wherein the interconnect route path comprises segments having different interconnect widths" (emphasis added).

Claim 9 recites "using *at least one flooding operation* to determine an interconnect route path between a first point and a second point of an integrated circuit design" (emphasis added).

Claim 13 recites "using *at least one flooding operation* to determine an interconnect route path between a first point and a second point of an integrated circuit design" (emphasis added).

Regarding a *shape-based automatic router tool* and *flooding operations*, the examiner's statement

> if a wire's or via's determined current density value exceeds its specified maximum allowable current density value, then the PG wiring analysis module 1007 increases the width of the wire or via to correct this

indicates a fundamental misunderstanding of the recited invention. One of skill in the art would understand the invention as recited. Some discussion of shaped-based routing and flooding is discussed in the application, for example, at paragraphs 29–30. The examiner *has not affirmatively described how any of the prior art references are relevant or related* to shape-based routing or flooding. In fact, the references are not.

Therefore, applicants *strongly maintain* that nowhere does Lin (or the other prior art references) show or suggest an automatic router tool using flood operations in creating an interconnect route path. Rather, Lin is a layout floor planning tool to optimize power and ground (PG) wires. Lin does not describe shaped-based automatic routing using flood operations. Lin and other prior art does not show or suggest the present invention and does not provide the features of the invention.

For at least this reason claims 1, 9, and 13 should be allowable. Claims 2–5, 7–8, and 21–22 are dependent on claim 1 and should be allowable for at least similar reasons as claim 1. Claim 10–12 are dependent on claim 9 and should be allowable for at least similar reasons as claim 9. Claim 14 is dependent on claim 13 and should be allowable for at least similar reasons as claim 13. The dependent claims recite additional limitations and should be further allowable because of these limitations.

Claims 23–29 also recites a "shape-based automatic router tool" and these claims should be allowable for similar reasons as discussed.

Claim 30 is not shown or suggested by Lin and Tripathi. Lin is inappropriate for at least reasons as has been described in the record. Tripathi is also completely inappropriate, and should not be combined with Lin. Tripathi is concerned with the mask or metallization layer (which occurs during mask making or fabrication), while the invention concerned with the computer aided design. Each particular step in the process of making an integrated circuit is independent from other steps; data available at one step may not be available at another step (or other cannot be used at another step). For example, during mask making step, information concerning connectivity and a interconnect route path is not available and wholly inappropriate.

The examiner does not appear to fully appreciate the *technicalities* or *technical difficulties* of creating a technique of the invention, which cannot be obtained by haphazard pinning together of the prior art references as the examiner has done. The *technical difficulties* and problems solved by the invention are those that *cannot be solved by simply cutting and pasting* bits and pieces from here and there together. It is not clear how the references can be combined to make the invention, especially in this case because it *not technically feasible* to do what the examiner asserts.

For at least this reason, claim 30 should be allowable.

Conclusion

For the above reasons, applicants believe all claims now pending in this application are in condition for allowance. Applicants respectfully request that a timely Notice of Allowance be issued in this case. If the examiner believes a telephone conference would expedite prosecution of this application, please contact the signee.

Respectfully submitted,

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